Claims

[c1] 1.A protection circuit for an integrated circuit device that includes silicon over insulator (SOI) transistors, wherein said protection circuit comprises:

a shunt connected to at least one of the source/drain and gate of at least one SOI transistor,

wherein said shunt eliminates the potential for charging damage to the gate insulator of said SOI transistor, and

wherein said shunt performs no function other than eliminating said potential for charging damage.

[c2] 2.The circuit in claim 1, wherein said shunt device is positioned in parallel with said SOI transistor.

[c3] 3.The circuit in claim 1, wherein said shunt device is positioned between a first conductor connected to said source/drain of said SOI transistor and a second conductor connected to said gate of said SOI transistor.

[c4] 4.The circuit in claim 1, further comprising a series device in place of said shunt.

[c5] 5.The circuit in claim 4, wherein said series device is positioned between a first conductor connected to said SOI

transistor and a second conductor that is not connected to said SOI transistor.

[c6] 6.The circuit in claim 4, further comprising a second series device, wherein said series device is connected to a first conductor and said second series device is connected to a second conductor, and
wherein said first conductor is connected to said source/drain of said SOI transistor and said second conductor is connected to said gate of said SOI transistor.

[c7] 7.A protection circuit for an integrated circuit device that includes silicon over insulator (SOI) transistors, wherein said protection circuit comprises:

a series device connected to at least one of the source/drain and gate of at least one SOI transistor; and

a compensating conductor connected to said series device,

wherein said series device and said compensating conductor eliminate the potential for charging damage between said source/drain and said gate of said SOI transistor, and

wherein said series device performs no function other than eliminating said potential for charging damage.

[c8] 8.The circuit in claim 7, wherein said series device is positioned in parallel with said SOI transistor.

[c9] 9.The circuit in claim 7, wherein said series device is positioned between a first conductor connected to said source/drain of said SOI transistor and a second conductor connected to said gate of said SOI transistor.

[c10] 10.The circuit in claim 7, wherein said series device comprises a diode.

[c11] 11.The circuit in claim 7, wherein said series device is positioned between a first conductor connected to said SOI transistor and a second conductor that is not connected to said SOI transistor.

[c12] 12.The circuit in claim 7, further comprising a second series device, wherein said series device is connected to a first conductor and said second series device is connected to a second conductor, and
wherein said first conductor is connected to said source/drain of said SOI transistor and said second conductor is connected to said gate of said SOI transistor.

[c13] 13.A protection circuit for an integrated circuit device that includes silicon over insulator (SOI) transistors, wherein said protection circuit comprises:
a shunt device connected to at least one of the

source/drain and gate of at least one SOI transistor, wherein said shunt device eliminates the potential for charging damage between said source/drain and said gate of said SOI transistor.

[c14] 14.The circuit in claim 13, wherein said shunt device is positioned in parallel with said SOI transistor.

[c15] 15.The circuit in claim 13, wherein said shunt device is positioned between a first conductor connected to said source/drain of said SOI transistor and a second conductor connected to said gate of said SOI transistor.

[c16] 16.The circuit in claim 13, wherein said shunt device comprises a diode.

[c17] 17.The circuit in claim 13, wherein said shunt device is positioned between a first conductor connected to said SOI transistor and a second conductor that is not connected to said SOI transistor.

[c18] 18.The circuit in claim 13, further comprising a second shunt device, wherein said shunt device is connected to a first conductor and said second shunt device is connected to a second conductor, and
wherein said first conductor is connected to said source/drain of said SOI transistor and said second conductor is connected to said gate of said SOI transistor.

[c19] 19.A protection circuit for an integrated circuit device that includes silicon over insulator (SOI) transistors, wherein said protection circuit comprises:

a series device connected to at least one of the source/drain and gate of at least one SOI transistor; and

a compensating conductor connected to said series device,

wherein said series device and said compensating conductor eliminate the potential for charging damage between said source/drain and said gate of said SOI transistor.

[c20] 20.The circuit in claim 19, wherein said series device is positioned in parallel with said SOI transistor.

[c21] 21.The circuit in claim 19, wherein said series device is positioned between a first conductor connected to said source/drain of said SOI transistor and a second conductor connected to said gate of said SOI transistor.

[c22] 22.The circuit in claim 19, wherein said series device comprises a diode.

[c23] 23.The circuit in claim 19, wherein said series device is positioned between a first conductor connected to said SOI transistor and a second conductor that is not con-

nected to said SOI transistor.

[c24] 24.The circuit in claim 19, further comprising a second series device, wherein said series device is connected to a first conductor and said second series device is connected to a second conductor, and
wherein said first conductor is connected to said source/drain of said SOI transistor and said second conductor is connected to said gate of said SOI transistor.

[c25] 25.A method of altering an integrated circuit design having silicon over insulator (SOI) transistors, wherein said method prevents damage from charge coupling between the source/drain and gate of SOI transistors, and
wherein said method comprises:

tracing electrical nets in said integrated circuit design;

identifying SOI transistors that have a voltage differential between the source/drain and gate as potentially damaged SOI transistors, based on said tracing of said electrical nets; and

connecting a shunt device to one of said source/drain and said gate of each of said potentially damaged SOI transistors to eliminate the potential for charging damage.

[c26] 26.The method in claim 25, wherein said tracing process

is performed assuming all metals and diffusions are conductive.

[c27] 27.The method in claim 25, wherein said identifying process comprises comparing aspect ratios of vias connected to said source/drain and said gate of each of said SOI transistors to determine whether a voltage differential may exist between said source/drain and said gate.

[c28] 28.The method in claim 25, wherein said identifying process comprises comparing chip locations of conductors connected to said source/drain and said gate of each of said SOI transistors to determine whether a voltage differential may exist between said source/drain and said gate.

[c29] 29.The method in claim 25, wherein said identifying process comprises comparing parasitic capacitances of conductors connected to said source/drain and said gate of each of said SOI transistors to determine whether a voltage differential may exist between said source/drain and said gate.

[c30] 30. The method in claim 25, wherein said tracing, said identifying, and said connecting are repeated for at each level of wiring within said integrated circuit design.

[c31] 31.A method of altering an integrated circuit design hav-

ing silicon over insulator (SOI) transistors, wherein said method prevents damage from charge coupling between the source/drain and gate of SOI transistors, and wherein said method comprises:

tracing electrical nets in said integrated circuit design;

identifying SOI transistors that have a voltage differential between the source/drain and gate as potentially damaged SOI transistors, based on said tracing of said electrical nets;

connecting a series device to one of said source/drain and said gate of each of said potentially damaged SOI transistors; and

connecting a compensating conductor to said series device,

wherein said series device and said compensating conductor eliminate the potential for charging damage between said source/drain and said gate of each of said potentially damaged SOI transistors.

[c32] 32.The method in claim 31, wherein said tracing process is performed assuming all metals and diffusions are conductive.

[c33] 33.The method in claim 31, wherein said identifying process comprises comparing aspect ratios of vias connected to said source/drain and said gate of each of said

SOI transistors to determine whether a voltage differential may exist between said source/drain and said gate.

[c34] 34.The method in claim 31, wherein said identifying process comprises comparing chip locations of conductors connected to said source/drain and said gate of each of said SOI transistors to determine whether a voltage differential may exist between said source/drain and said gate.

[c35] 35.The method in claim 31, wherein said identifying process comprises comparing parasitic capacitances of conductors connected to said source/drain and said gate of each of said SOI transistors to determine whether a voltage differential may exist between said source/drain and said gate.

[c36] 36. The method in claim 31, wherein said tracing, said identifying, and said connecting processes are repeated at each level of wiring within said integrated circuit design.